ACADEMIC REGULATIONS
COURSE STRUCTURE
AND
DETAILED SYLLABUS

For

ECE BRANCH

COMMON FOR

VLSI&ES, ES&VLSI, VLSID&ES

JAWAHARLAL NEHRU TECHNOLOGY UNIVERSITY KAKINADA

KAKINADA - 533 003, Andhra Pradesh, India

ACADEMIC REGULATIONS R13 FOR M. Tech (REGULAR) DEGREE COURSE

Applicable for the students of M. Tech (Regular) Course from the Academic Year 2013-14 onwards

The M. Tech Degree of Jawaharlal Nehru Technological University Kakinada shall be conferred on candidates who are admitted to the program and who fulfil all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the University or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Govt. from time to time.

2.0 AWARD OF M. Tech DEGREE

2.1 A student shall be declared eligible for the award of the M. Tech Degree, if he pursues a course of study in not less than two and not more than four academic years.

2.2 The student shall register for all 80 credits and secure all the 80 credits.

2.3 The minimum instruction days in each semester are 90.

3.0 A. COURSES OF STUDY

The following specializations are offered at present for the M. Tech course of study.

1. M.Tech- Structural Engineering
2. M.Tech- Transportation Engineering
3. M.Tech- Infrastructure Engineering & Management
4. ME- Soil Mechanics and Foundation Engineering
5. M.Tech- Environmental Engineering
6. M.Tech-Geo-Informatics
7. M.Tech-Spatial Information Technology

8. M.Tech- Civil Engineering
9. M.Tech -Geo-Technical Engineering
10. M.Tech- Remote Sensing
11. M.Tech- Power Electronics
12. M.Tech- Power & Industrial Drives
13. M.Tech- Power Electronics & Electrical Drives
14. M.Tech- Power System Control & Automation
15. M.Tech- Power Electronics & Drives
16. M.Tech- Power Systems
17. M.Tech- Power Systems Engineering
18. M.Tech- High Voltage Engineering
19. M.Tech- Power Electronics and Power Systems
20. M.Tech- Power System and Control
21. M.Tech- Power Electronics & Systems
22. M.Tech- Electrical Machines and Drives
23. M.Tech- Advanced Power Systems
24. M.Tech- Power Systems with Emphasis on High Voltage Engineering
25. M.Tech- Control Engineering
26. M.Tech- Control Systems
27. M.Tech- Electrical Power Engineering
28. M.Tech- Power Engineering & Energy System
29. M.Tech- Thermal Engineering
30. M.Tech- CAD/CAM
31. M.Tech- Machine Design
32. M.Tech- Computer Aided Design and Manufacture
33. M.Tech- Advanced Manufacturing Systems
34. M.Tech-Computer Aided Analysis & Design
35. M.Tech- Mechanical Engineering Design
36. M.Tech- Systems and Signal Processing
37. M.Tech- Digital Electronics and Communication Systems
38. M.Tech- Electronics & Communications Engineering
39. M.Tech- Communication Systems
40. M.Tech- Communication Engineering & Signal Processing
41. M.Tech- Microwave and Communication Engineering
42. M.Tech- Telematics

43. M.Tech- Digital Systems & Computer Electronics
44. M.Tech- Embedded System
45. M.Tech- VLSI
46. M.Tech- VLSI Design
47. M.Tech- VLSI System Design
48. M.Tech- Embedded System & VLSI Design
49. M.Tech- VLSI & Embedded System
50. M.Tech- VLSI Design & Embedded Systems
51. M.Tech- Image Processing
52. M.Tech- Digital Image Processing
53. M.Tech- Computers & Communication
54. M.Tech- Computers & Communication Engineering
55. M.Tech- Instrumentation & Control Systems
56. M.Tech – VLSI & Micro Electronics
57. M.Tech – Digital Electronics & Communication Engineering
58. M.Tech- Embedded System & VLSI
59. M.Tech- Computer Science & Engineering
60. M.Tech- Computer Science
61. M.Tech- Computer Science & Technology
62. M.Tech- Computer Networks
63. M.Tech- Computer Networks & Information Security
64. M.Tech- Information Technology
65. M.Tech- Software Engineering
66. M.Tech- Neural Networks
67. M.Tech- Chemical Engineering
68. M.Tech- Biotechnology
69. M.Tech- Nano Technology
70. M.Tech- Food Processing
71. M.Tech- Avionics

and any other course as approved by AICTE/ University from time to time.

3.0 B. Departments offering M. Tech Programmes with specializations are noted below:

Civil Engg.	1. M.Tech- Structural Engineering 2. M.Tech- Transportation Engineering 3. M.Tech- Infrastructure Engineering & Management 4. ME- Soil Mechanics and Foundation Engineering 5. M.Tech- Environmental Engineering 6. M.Tech-Geo-Informatics 7. M.Tech-Spatial Information Technology 8. M.Tech- Civil Engineering 9. M.Tech -Geo-Technical Engineering 10. M.Tech- Remote Sensing
EEE	1. M.Tech- Power Electronics 2. M.Tech- Power & Industrial Drives 3. M.Tech- Power Electronics & Electrical Drives 4. M.Tech- Power System Control & Automation 5. M.Tech- Power Electronics & Drives 6. M.Tech- Power Systems 7. M.Tech- Power Systems Engineering 8. M.Tech- High Voltage Engineering 9. M.Tech- Power Electronics and Power Systems 10. M.Tech- Power System and Control 11. M.Tech- Power Electronics & Systems 12. M.Tech- Electrical Machines and Drives 13. M.Tech- Advanced Power Systems 14. M.Tech- Power Systems with Emphasis on High Voltage Engineering 15. M.Tech- Control Engineering 16. M.Tech- Control Systems 17. M.Tech- Electrical Power Engineering 18. M.Tech- Power Engineering & Energy System
ME	1. M.Tech- Thermal Engineering 2. M.Tech- CAD/CAM 3. M.Tech- Machine Design 4. M.Tech- Computer Aided Design and Manufacture 5. M.Tech- Advanced Manufacturing Systems 6. M.Tech-Computer Aided Analysis & Design 7. M.Tech- Mechanical Engineering Design

ECE	1. M.Tech- Systems and Signal Processing 2. M.Tech- Digital Electronics and Communication Systems 3. M.Tech- Electronics & Communications Engineering 4. M.Tech- Communication Systems 5. M.Tech- Communication Engineering & Signal Processing 6. M.Tech- Microwave and Communication Engineering 7. M.Tech- Telematics 8. M.Tech- Digital Systems & Computer Electronics 9. M.Tech- Embedded System 10. M.Tech- VLSI 11. M.Tech- VLSI Design 12. M.Tech- VLSI System Design 13. M.Tech- Embedded System & VLSI Design 14. M.Tech- VLSI & Embedded System 15. M.Tech- VLSI Design & Embedded Systems 16. M.Tech- Image Processing 17. M.Tech- Digital Image Processing 18. M.Tech- Computers & Communication 19. M.Tech- Computers & Communication Engineering 20. M.Tech- Instrumentation & Control Systems 21. M.Tech – VLSI & Micro Electronics 22. M.Tech – Digital Electronics & Communication Engineering 23. M.Tech- Embedded System & VLSI
CSE	1. M.Tech- Computer Science & Engineering 2. M.Tech- Computer Science 3. M.Tech- Computer Science & Technology 4. M.Tech- Computer Networks 5. M.Tech- Computer Networks & Information Security 6. M.Tech- Information Technology 7. M.Tech- Software Engineering 8. M.Tech- Neural Networks
Others	1. M.Tech- Chemical Engineering 2. M.Tech- Biotechnology 3. M.Tech- Nano Technology 4. M.Tech- Food Processing 5. M.Tech- Avionics

4.0 ATTENDANCE

4.1 A student shall be eligible to write University examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

4.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester shall be granted by the College Academic Committee.

4.3 Shortage of Attendance below 65% in aggregate shall not be condoned.

4.4 Students whose shortage of attendance is not condoned in any semester are not eligible to write their end semester examination of that class.

4.5 A prescribed fee shall be payable towards condonation of shortage of attendance.

4.6 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

5.0 EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

5.1 For the theory subjects 60 marks shall be awarded based on the performance in the End Semester Examination and 40 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be made based on the **average** of the marks secured in the two Mid Term-Examinations conducted-one in the middle of the Semester and the other immediately after the completion of instruction. Each mid term examination shall be conducted for a total duration of 120 minutes with 4 questions (without choice) each question for 10 marks. End semester examination is conducted for 60 marks for 5 questions to be answered out of 8 questions.

5.2 For practical subjects, 60 marks shall be awarded based on the performance in the End Semester Examinations and 40 marks shall be awarded based on the day-to-day performance as Internal Marks.

5.3 There shall be two seminar presentations during III semester and IV semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.4 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.5 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.4) he has to reappear for the End semester Examination in that subject. A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and has failed in the end examination. In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled. For re-registration the candidates have to apply to the University through the college by paying the requisite fees and get approval from the University before the start of the semester in which re-registration is required.

5.6 In case the candidate secures less than the required attendance in any re registered subject (s), he shall not be permitted to write the End Examination in that subject. He shall again re-register the subject when next offered.

5.7 Laboratory examination for M. Tech. courses must be conducted with two Examiners, one of them being the Laboratory Class Teacher or teacher of the respective college and the second examiner shall be appointed by the university from the panel of examiners submitted by the respective college.

6.0 EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

6.1 A Project Review Committee (PRC) shall be constituted with Head of the Department and two other senior faculty members.

6.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work for approval. The student can initiate the Project work, only after obtaining the approval from the Project Review Committee (PRC).

6.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the Project Review Committee (PRC). However, the Project Review Committee (PRC) shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.5 A candidate shall submit his status report in two stages at least with a gap of 3 months between them.

6.6 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after

successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. The candidate has to pass all the theory and practical subjects before submission of the Thesis.

6.7 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/School/Institute.

6.8 The thesis shall be adjudicated by one examiner selected by the University. For this, the Principal of the College shall submit a panel of 5 examiners, eminent in that field, with the help of the guide concerned and head of the department.

6.9 If the report of the examiner is not favourable, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the University.

6.10 If the report of the examiner is favourable, Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Board shall jointly report the candidate's work as one of the following:

A. Excellent
B. Good
C. Satisfactory
D. Unsatisfactory

The Head of the Department shall coordinate and make arrangements for the conduct of Viva-Voce examination.

6.11 If the report of the Viva-Voce is unsatisfactory, the candidate shall retake the Viva-Voce examination only after three months. If he fails to get a satisfactory report at the second Viva-Voce examination, the candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the University.

7.0 AWARD OF DEGREE AND CLASS

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following four classes:

Class Awarded	**% of marks to be secured**
First Class with Distinction	70% and above (Without any Supplementary Appearance)
First Class	Below 70% but not less than 60% 70% and above (With any Supplementary Appearance)
Second Class	Below 60% but not less than 50%

The marks in internal evaluation and end examination shall be shown separately in the memorandum of marks.

8.0 WITHHOLDING OF RESULTS

If the student has not paid the dues, if any, to the university or if any case of indiscipline is pending against him, the result of the student will be withheld. His degree will be withheld in such cases.

4.0 TRANSITORY REGULATIONS (for R09)

9.1 Discontinued or detained candidates are eligible for re-admission into same or equivalent subjects at a time as and when offered.

9.2 The candidate who fails in any subject will be given two chances to pass the same subject; otherwise, he has to identify an equivalent subject as per R13 academic regulations.

10. GENERAL

10.1 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

10.2 The academic regulation should be read as a whole for the purpose of any interpretation.

10.3 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.

10.4 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the University.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/ Improper conduct	Punishment
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project

	(theory or practical) in which the candidate is appearing.	work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and

	the examination.	shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/ Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.

	outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining

		examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/ year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions : (if the squad reports that the college is also involved in encouraging malpractices)
   - (i) A show cause notice shall be issued to the college.
   - (ii) Impose a suitable fine on the college.
   - (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA

KAKINADA-533003, Andhra Pradesh (India)
For Constituent Colleges and Affiliated Colleges of JNTUK

Ragging

Prohibition of ragging in educational institutions Act 26 of 1997

Salient Features

- ⇨ Ragging within or outside any educational institution is prohibited.
- ⇨ Ragging means doing an act which causes or is likely to cause Insult or Annoyance of Fear or Apprehension or Threat or Intimidation or outrage of modesty or Injury to a student

	Imprisonment upto		Fine Upto
Teasing, Embarrassing and Humiliation	6 Months	+	Rs. 1,000/-
Assaulting or Using Criminal force or Criminal intimidation	1 Year	+	Rs. 2,000/-
Wrongfully restraining or confining or causing hurt	2 Years	+	Rs. 5,000/-
Causing grievous hurt, kidnapping or Abducts or rape or committing unnatural offence	5 Years	+	Rs.10,000/-
Causing death or abetting suicide	10 Months	+	Rs. 50,000/-

In Case of Emergency CALL TOLL FREE NO. : 1800 - 425 - 1288

LET US MAKE JNTUK A RAGGING FREE UNIVERSITY

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA

KAKINADA-533003, Andhra Pradesh (India)
For Constituent Colleges and Affiliated Colleges of JNTUK

Ragging

ABSOLUTELY NO TO RAGGING

1. Ragging is prohibited as per Act 26 of A.P. Legislative Assembly, 1997.
2. Ragging entails heavy fines and/or imprisonment.
3. Ragging invokes suspension and dismissal from the College.
4. Outsiders are prohibited from entering the College and Hostel without permission.
5. Girl students must be in their hostel rooms by 7.00 p.m.
6. All the students must carry their Identity Card and show them when demanded
7. The Principal and the Wardens may visit the Hostels and inspect the rooms any time.

Jawaharlal Nehru Technological University Kakinada
For Constituent Colleges and Affiliated Colleges of JNTUK

In Case of Emergency CALL TOLL FREE NO. : 1800 - 425 - 1288

LET US MAKE JNTUK A RAGGING FREE UNIVERSITY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Specialization: VLSI&ES, ES&VLSI, VLSID&ES

COURSE STRUCTURE

I SEMESTER

S.No	Name of the Subject	L	P	C
1	Microcontrollers for Embedded System Design	4	-	3
2	VLSI Technology and Design	4	-	3
3	CMOS Analog IC Design	4	-	3
4	CPLD and FPGA Architectures and Applications	4	-	3
5	**Elective I** Hardware Software Co-Design Digital System Design Soft Computing Techniques	4	-	3
6	**Elective II** Advanced Operating Systems CMOS Digital IC Design Network Security and Cryptography.	4	-	3
7	**Laboratory** VLSI Laboratory	-	3	2
	TOTAL			**20**

II SEMESTER

1	Embedded - C	4	-	3
2	CMOS Mixed Signal Circuit Design	4	-	3
3	Embedded Real Time Operating Systems	4	-	3
4	Design For Testability	4	-	3
5	**Elective III** Digital Signal Processors & Architectures System on Chip Design VLSI Signal Processing	4	-	3
6	**Elective IV**			
	Micro Electro Mechanical Systems (MEMS) Design Low Power VLSI Design Semiconductor Memory Design and Testing	4	-	3
7	**Laboratory** Embedded Systems Laboratory	-	3	2
	TOTAL			**20**

III – SEMESTER

1	Seminar	—	—	2
2	Project	—	—	18
	Total			**20**

IV – SEMESTER

1	Seminar	—	—	2
2	Project (Continued)	—	—	18
	Total			**20**

The project will be evaluated at the end of the IV Semester

SYLLABUS

I – I	L	P	Credits
	4	-	3

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

UNIT-I

ARM Architecture ARM Design Philosophy, Registers, PSR, Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT-II

ARM Programming Model-I Instruction Set: Data Processing Instructions, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT-III

ARM Programming Model-II Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions.

UNIT-IV

ARM Programming Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT-V

Memory Management Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Content Switch.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

I – I	L	P	Credits
	4	-	3
VLSI TECHNOLOGY AND DESIGN			

UNIT-I

VLSI Technology: Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters.

VLSI Design: Electronic design automation concept, ASIC and FPGA design flows, SOC designs, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues.

UNIT-II

CMOS VLSI Design: MOS Technology and fabrication process of pMOS, nMOS, CMOS and BiCMOS technologies**,** comparison of different processes.

Building Blocks of a VLSI circuit: Computer architecture, memory architectures, communication interfaces, mixed signal interfaces.

VLSI Design Issues: Design process, design for testability, technology options, power calculations, package selection, clock mechanisms, mixed signal design.

UNIT-III

Basic electrical properties of MOS and BiCMOS circuits, MOS and BiCMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitatitive and quantitative analysis with proper illustrations and necessary derivations of expressions.

UNIT-IV

Subsystem Design and Layout: Some architectural issues, switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations.

Subsystem Design Processes: Some general considerations and an illustration of design processes, design of an ALU subsystem.

UNIT-V

Floor Planning: Introduction**,** Floor planning methods, off-chip connections.

Architecture Design: Introduction, Register-Transfer design, high-level synthesis, architectures for low power, architecture testing.

Chip Design: Introduction and design methodologies.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A. Pucknell, Sholeh Eshraghian, 2005, PHI Publications.
2. Modern VLSI Design-Wayne Wolf, 3rd Ed., 1997, Pearson Education.
3. VLSI Design-Dr.K.V.K.K.Prasad, Kattula Shyamala, Kogent Learning Solutions Inc., 2012.

REFERENCE BOOKS:

1. VLSI Design Technologies for Analog and Digital Circuits, Randall L.Geiger, Phillip E.Allen, Noel R.Strader, TMH Publications, 2010.
2. Introduction to VLSI Systems: A Logic, Circuit and System Perspective-Ming-BO Lin, CRC Press, 2011.
3. Principals of CMOS VLSI Design-N.H.E Weste, K. Eshraghian, 2nd Edition, Addison Wesley.

I – I	L	P	Credits
	4	-	3
CMOS ANALOG IC DESIGN			

Specialization: VLSI/ VLSI Design/ VLSI System Design

UNIT –I

MOS Devices and Modeling The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT –II

Analog CMOS Sub-Circuits MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT –III

CMOS Amplifiers Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT –IV

CMOS Operational Amplifiers Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT –V

Comparators Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn, 2013.

2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.

3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

I – I	L	P	Credits
	4	-	3

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

UNIT-I

Introduction to Programmable Logic Devices Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/ Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II

Field Programmable Gate Arrays Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT –III

SRAM Programmable FPGAs Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT –IV

Anti-Fuse Programmed FPGAs Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT –V

Design Applications General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.

2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.

2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/ Samiha Mourad, Pearson Low Price Edition.

3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.

4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

I – I	L	P	Credits
	4	-	3

(ELECTIVE-I)
HARDWARE SOFTWARE CO-DESIGN

UNIT-I

Co- Design Issues Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT-II

Prototyping and Emulation Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-III

Compilation Techniques and Tools for Embedded Processor Architectures

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT-IV

Design Specification and Verification Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT-V

Languages for System-Level Specification and Design-I System-level specification, design representation for system level synthesis, system level specification languages.

Languages for System-Level Specification and Design-II Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer Publications.

I – I	L	P	Credits
	4	-	3

(ELECTIVE-I)
DIGITAL SYSTEM DESIGN

UNIT-I

Minimization Procedures and CAMP Algorithm Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs,, CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-II

PLA Design, PLA Minimization and Folding Algorithms Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm(IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT –III

Design of Large Scale Digital Systems Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-IV

Fault Diagnosis in Combinational Circuits Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT-V

Fault Diagnosis in Sequential Circuits Fault detection and location in sequential circuits, circuit test approach, initial state identification, Haming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

TEXT BOOKS:

1. Logic Design Theory-N. N. Biswas, PHI
2. Switching and Finite Automata Theory-Z. Kohavi , 2nd Edition, 2001, TMH
3. Digital system Design using PLDd-Lala

REFERENCE BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.

I – I	L	P	Credits
	4	-	3

(ELECTIVE-I)
SOFT COMPUTING TECHNIQUES

UNIT –I

Introduction: Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT –II

Artificial Neural Networks: Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –III

Fuzzy Logic System: Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –IV

Genetic Algorithm: Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and anD-colony search techniques for solving optimization problems.

UNIT –V

Applications: GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis

of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

TEXT BOOKS:

1. Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999.
2. Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994.

REFERENCE BOOKS:

1. Fuzzy Sets, Uncertainty and Information - Klir G.J. & Folger T.A., Prentice-Hall of India Pvt. Ltd., 1993.
2. Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994.
3. Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers.
4. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
5. Elements of Artificial Neural Networks - Kishan Mehrotra, Chelkuri K. Mohan, Sanjay Ranka, Penram International.
6. Artificial Neural Network –Simon Haykin, 2nd Ed., Pearson Education.
7. Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi.

I – I	L	P	Credits
	4	-	3

(ELECTIVE-II)
ADVANCED OPERATING SYSTEMS

UNIT-I

Introduction to Operating Systems Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT-II

Introduction to UNIX and LINUX Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations

UNIT –III

System Calls: System calls and related file structures, Input / Output, Process creation & termination.

Inter Process Communication : Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV

Introduction to Distributed Systems: Goals of distributed system, Hardware and software concepts, Design issues.

Communication in Distributed Systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V

Synchronization in Distributed Systems: Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions

Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:

1. The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete Reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.

REFERENCE BOOKS:

1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems - Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles - Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens, 1998, PHI.

I – I	L	P	Credits
	4	-	3

(ELECTIVE-II)
CMOS DIGITAL IC DESIGN

UNIT-I

MOS Design Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III

Sequential MOS Logic Circuits Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-IV

Dynamic Logic Circuits Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V

Semiconductor Memories Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.

2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

I – I	L	P	Credits
	4	-	3

(ELECTIVE-II)
NETWORK SECURITY & CRYPTOGRAPHY

UNIT-I

Introduction Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security.Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT-II

Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT-III

Number Theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

Message authentication and Hash Functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT-IV

Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC.

Digital signatures and Authentication Protocols: Digital signatures, Authentication Protocols, Digital signature standards.

Authentication Applications: Kerberos, X.509 directory Authentication service.Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT-V

IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.

Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction.

Intruders, Viruses and Worms: Intruders, Viruses and Related threats.

Fire Walls: Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

1. Cryptography and Network Security: Principles and Practice - William Stallings, 2000, PE.

REFERENCE BOOKS:

1. Principles of Network and Systems Administration, Mark Burgess,John Wiey.

I – I	L	P	Credits
	-	3	2
VLSI LABORATORY			

PART-A: VLSI Lab (Front-end Environment)

- **The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/ Mentor Graphics Questa Simulator) to verify the logical / functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).**
- **The students are required to acquire the knowledge in both the Platforms (Xilinx and Mentor graphics) by perform at least SIX experiments on each Platform.**

List of Experiments:

1. Realization of Logic gates.
2. Parity Encoder.
3. Random Counter
4. Synchronous RAM.
5. ALU.
6. UART Model.
7. Fire Detection and Control System using Combinational Logic circuits.
8. Traffic Light Controller using Sequential Logic circuits
9. Pattern Detection using Moore Machine.
10. Finite State Machine (FSM) based logic circuit.

PART-A: VLSI Lab (Back-end Environment)

- **The students are required to design and implement the Layout of the following experiments of any FOUR using CMOS 130nm Technology with Mentor Graphics Tool.**

List of Experiments:

1. Inverter Characteristics.
2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter.
5. Static and Dynamic RAM.
6. ROM
7. Digital-to-Analog-Converter.
8. Analog-to-Digital Converter.

Lab Requirements:

Software:

Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Mentor Graphics Back End/Tanner Software tool.

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

I – II	L	P	Credits
	4	-	3
EMBEDDED C			

UNIT-I

Programming Embedded Systems in C Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements, Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption, Conclusions

UNIT-II

Reading Switches Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT-III

Adding Structure to the Code Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT-IV

Meeting Real-Time Constraints Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example:

Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT-V

Case Study-Intruder Alarm System Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:

1. Embedded C - Michael J. Pont, 2nd Ed., Pearson Education, 2008.

REFERENCE BOOKS:

1. PIC MCU C-An introduction to programming, The Microchip PIC in CCS C - Nigel Gardner.

I – II	L	P	Credits
	4	-	3

CMOS MIXED SIGNAL CIRCUIT DESIGN

UNIT-I

Switched Capacitor Circuits Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT-II

Phased Lock Loop (PLL) Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III

Data Converter Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-IV

Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT-V

Oversampling Converters Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg,

Oxford University Press, International Second Edition/Indian Edition, 2010.

3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003

2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.

3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

I – II	L	P	Credits
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EMBEDDED REAL TIME OPERATING SYSTEMS

UNIT-I

Introduction OS Services, Process Management, Timer Functions, Event Functions, Memory Management, Device, File and IO Systems Management, Interrupt Routines in RTOS Environment and Handling of Interrupt Source Calls, Real-Time Operating Systems, Basic Design Using an RTOS, RTOS Task Scheduling Models, Interrupt Latency and Response of the Tasks as Performance Metrics, OS Security Issues.

UNIT-II

RTOS Programming Basic Functions and Types of RTOS for Embedded Systems, RTOS mCOS-II, RTOS Vx Works, Programming concepts of above RTOS with relevant Examples, Programming concepts of RTOS Windows CE, RTOS OSEK, RTOS Linux 2.6.x and RTOS RT Linux.

UNIT-III

Program Modeling – Case Studies Case study of embedded system design and coding for an Automatic Chocolate Vending Machine (ACVM) Using Mucos RTOS, case study of digital camera hardware and software architecture, case study of coding for sending application layer byte streams on a TCP/IP Network Using RTOS Vx Works, Case Study of Embedded System for an Adaptive Cruise Control (ACC) System in Car, Case Study of Embedded System for a Smart Card, Case Study of Embedded System of Mobile Phone Software for Key Inputs.

UNIT-IV

Target Image Creation & Programming in Linux Off-The-Shelf Operating Systems, Operating System Software, Target Image Creation for Window XP Embedded, Porting RTOS on a Micro Controller based Development Board.Overview and programming concepts of Unix/Linux Programming, Shell Programming, System Programming.

UNIT-V

Programming in RT Linux Overview of RT Linux, Core RT Linux API, Program to display a message periodically, semaphore management, Mutex, Management, Case Study of Appliance Control by RT Linux System.

TEXT BOOKS:

1. Dr. K.V.K.K. Prasad: "Embedded/Real-Time Systems" Dream Tech Publications, Black pad book.
2. Rajkamal: "Embedded Systems-Architecture, Programming and Design", Tata McGraw Hill Publications, Second Edition, 2008.

REFERENCES:

Labrosse, "Embedding system building blocks ", CMP publishers.

1. Rob Williams," Real time Systems Development", Butterworth Heinemann Publications.

I – II	L	P	Credits
	4	-	3

DESIGN FOR TESTABILITY

UNIT-I

Introduction to Testing Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II

Logic and Fault Simulation Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT –III

Testability Measures SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV

Built-In Self-Test The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V

`Boundary Scan Standard Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

I – II	L	P	Credits
	4	-	3

(ELECTIVE-III)
DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

UNIT-I

Introduction to Digital Signal Processing Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT-II

Architectures for Programmable DSP Devices Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT-III

Programmable Digital Signal Processors Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT-IV

Analog Devices Family of DSP Devices Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.

Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT-V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications- B. Venkataramani and M. Bhaskar, 2002, TMH.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
3. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
4. *The Scientist and Engineer's Guide to Digital Signal Processing* by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997

I – II	L	P	Credits
	4	-	3

(ELECTIVE-III)
SYSTEM ON CHIP DESIGN

UNIT-I

Introduction to the System Approach

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT-II

Processors Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT-III

Memory Design for SOC Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT-IV

Interconnect Customization and Configuration Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT-V

Application Studies / Case Studies SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques – Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

I – II	L	P	Credits
	4	-	3

(ELECTIVE-III)
VLSI SIGNAL PROCESSING

UNIT-I

Introduction to DSP Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming

Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT-II

Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems

Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT-III

Systolic Architecture Design

Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT-IV

Fast Convolution Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT-V

Low Power Design Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches

Programmable DSP: Evaluation of Programmable Digital Signal

Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

I – II	L	P	Credits
	4	-	3

(ELECTIVE-IV)
MICRO ELECTRO MECHANICAL SYSTEM DESIGN

UNIT-I

Introduction Basic structures of MEM devices – (Canti-Levers, Fixed Beams diaphragms). Broad Response of Micro electromechanical systems (MEMS) to Mechanical (Force, pressure etc.) Thermal, Electrical, optical and magnetic stimuli, compatibility of MEMS from the point of power dissipation, leakage etc.

UNIT-II

Review Review of mechanical concepts like stress, strain, bending moment, deflection curve. Differential equations describing the deflection under concentrated force, Distributed force, distributed force, Deflection curves for canti-levers- fixed beam. Electrostatic excitation – columbic force between the fixed and moving electrodes. Deflection with voltage in C.L, Deflection Vs Voltage curve, critical fringe field – field calculations using Laplace equation. Discussion on the approximate solutions – Transient response of the MEMS.

UNIT-III

Types Two terminal MEMS - capacitance Vs voltage Curve – Variable capacitor. Applications of variable capacitors. Two terminal MEM structures. Three terminal MEM structures – Controlled variable capacitors – MEM as a switch and possible applications.

UNIT-IV

MEM Circuits & Structures MEM circuits & structures for simple GATES- AND, OR, NAND, NOR, Exclusive OR, simple MEM configurations for flip-flops triggering applications to counters, converters. Applications for analog circuits like frequency converters, wave shaping. RF Switches for modulation. MEM Transducers for pressure, force temperature. Optical MEMS.

UNIT-V

MEM Technologies Silicon based MEMS- Process flow – Brief account of various processes and layers like fixed layer, moving layers spacers etc., and etching technologies.

Metal Based MEMS: Thin and thick film technologies for MEMS. Process flow and description of the processes, Status of MEMS in the current electronics scenario.

TEXT BOOKS:

1. MEMS Theory, Design and Technology - GABRIEL. M.Review, R.F.,2003, John wiley & Sons. .
2. Strength of Materials –Thimo Shenko, 2000, CBS publishers & Distributors.
3. MEMS and NEMS, Systems Devices; and Structures - Servey E.Lyshevski, 2002, CRC Press.

REFERENCE BOOKS:

1. Sensor Technology and Devices - Ristic L. (Ed) , 1994, Artech House, London.

I – II	L	P	Credits
	4	-	3

(ELECTIVE-IV)
LOW POWER VLSI DESIGN

UNIT-I

Fundamentals of Low Power VLSI Design Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT-II

Low-Power Design Approaches Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT-III

Low-Voltage Low-Power Adders Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT-IV

Low-Voltage Low-Power Multipliers Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT-V

Low-Voltage Low-Power Memories Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power

SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
2. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
3. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
4. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.

I – II	L	P	Credits
	4	-	3

(ELECTIVE-IV)
SEMICONDUCTOR MEMORY DESIGN AND TESTING

UNIT-I

Random Access Memory Technologies SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT-II

Non-volatile Memories Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT-III

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance

RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT-IV

Semiconductor Memory Reliability and Radiation Effects General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and

Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT-V

Advanced Memory Technologies and High-density Memory Packing Technologies

Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.

I – II	L	P	Credits
	-	3	2
EMBEDDED SYSTEMS LABORATORY			

- **The Students are required to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits and ARM-Cortex.**
- **The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design.**
- **The students are required to perform at least SIX experiments from Part-I and TWO experiments from Part-II.**

List of Experiments:

Part-I:

Experiments using ARM-926 with PERFECT RTOS

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader's Writer's Problem for concurrent Tasks.

Part-II

Experiments on ARM-CORTEX processor using any open source RTOS.

(Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Interface ADC and DAC ports with the Input and Output sensitive devices.
3. Simulate the temperature DATA Logger with the SERIAL communication with PC.
4. Implement the developer board as a modem for data communication using serial port communication between two PC's.

Lab Requirements:

Software:

(i) Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO- COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.

(ii) LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

Hardware:

(i) The development kits of ARM-926 Developer Kits and ARM-Cortex Boards.

(ii) Serial Cables, Network Cables and recommended power supply for the board.